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Code No: A5704

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
M.TECH I SEMESTER EXAMINATIONS, APRIL/MAY-2012
ELECTRONIC DESIGN AUTOMATION TOOLS
(VLSI SYSTEM DESIGN)

Time: 3hours **Max.Marks:60**

Answer any five questions
All questions carry equal marks
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1.a) Describe about conditional, procedural, procedural continuous and non-blocking assignments with their syntaxes and examples.
b) Write verilog code for 4 to 1 multiplexer using procedural continuous assignments.

2.a) Discuss about event control, named events, intra-assignment delay and pin-to-pin delay timing controls with their syntaxes.
b) Write verilog code for d-type flip-flop with reset and set controls by incorporating synchronization controls.

3.a) With the help of neat block diagram describe the logic synthesis procedure and explain about each step.
b) Model a synthesizable RAM memory using verilog.

4.a) Explain about various simulations and their significance with the help of flow diagram.
b) Discuss about cell models, delay models available in verilog.

5.a) Write the spice syntax for the following
Transient analysis, ac analysis, noise analysis, Fourier analysis, operating point, sweep analysis, transfer function and sensitivity analysis with one example each.
b) Write spice code for op-amp based integrator to get transient response.

6.a) List out and explain different approaches for modeling the mixed signal circuits.
b) Model a ‘Digital to analog converter’ in mixed signal modeling.

7.a) Discuss various issues involved in high speed PCB design.
b) Explain about ‘ORCAD component information’ system with the help of neat block diagram.

8. Answer any two
a) Verilog operators.
b) Static timing analysis.
c) P-spice code for CMOS inverter.

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